Creating PCB Editor Net Classes from OrCAD Capture / CIS

In PCB Editor, Constraint sets defining Physical and Spacing rules can be assigned to individual nets, or groups of nets, called Net Classes. It can often be more convenient to manage the creation of Net Classes from the schematic, since the grouping of nets into Net Classes can be more easily identified there. The first section of this note describes how to add properties to nets in the schematic to control the creation of Physical and Spacing Net Classes when the netlist is imported into PCB Editor.

The Controlling Properties

NET_PHYSICAL_TYPE takes a name for the Net Class to be created in the Physical domain of the Constraint Manager. Nets with the same NET_PHYSICAL_TYPE will grouped into the same Net Class when the netlist is imported into PCB Editor. The Netlist / Back Annotation flow will automatically handle a “_PH” value appended to the user defined Net Class name to help avoid conflicts between Physical and Spacing Net Classes when the netlist is imported into PCB Editor.

NET_SPACING_TYPE takes a name for the Net Class to be created in the Spacing domain of the Constraint Manager. Again, Nets with the same NET_SPACING_TYPE will be grouped into the same Net Class when the netlist is imported into PCB Editor.

A Practical Example

Let’s take a look at assigning the properties to some nets in a schematic and see what Net Classes are created. For this example, NET_PHYSICAL_TYPEs of POWER will be added to the Power nets: VCC, GND, AGND, GND_EARTH, V+12, V12N; VDNETS will be added to nets VD0-7; and SYNC will be added to nets VCLKA and VCLKC.

NET_SPACING_TYPEs of OUTPUT will be added to nets OUTA and OUTB; and SYNC will be added nets VCLKA and VCLKC.

Assigning NET_PHYSICAL_TYPE

The DSN file is selected in the Project Window and Edit>Object properties used to open the Property Editor at the Design level. The Property Editor is switched to the Schematic Nets tab and the AGND net located.
POWER is added to the NET_PHYSICAL_TYPE property cell. IF the NET_PHYSICAL_TYPE is not listed in the “Current Properties” filter, switch the “Filter by:” to “Cadence-Allegro”, locate the NET_PHYSICAL_TYPE property cell and set the value. The process is repeated for the other Nets that need the NET_PHYSICAL_TYPEs added. The NET_SPACING_TYPEs are added in a similar fashion but the NET_SPACING_TYPE cell is used instead.

(The NET_PHYSICAL_TYPE / NET_SPACING_TYPE can also be added by double-clicking on the net in the schematic. Be aware that this assigns the property to “that net” in “that schematic” so there is the possibility of assigning conflicting values unless some care is applied)

Generating the netlist

After checking for any design rule violations, Tools - Create Netlist is used to create the netlist. In this case a master board in the current schematic design directory is used as the starting point and the resulting board created with the netlist loaded as “start.brd” in the “allegro” directory beneath the current schematic design directory, and the board opened in PCB Editor.

Checking the Physical Net Classes created in PCB Editor

In PCB Editor, the Constraint Manager is opened; Setup – Constraints - Physical will open the Constraint Manager with the Physical domain active. The Net / All Layers entry is selected on the left hand side and the nets appear as follows:
Note that the Net Classes POWER_PH, SYNC_PH and VDNETS_PH have been created. The numbers after the Net Class names indicate the number of members of the Net Class and the “+” next to the Net Class name can be clicked to view the members:

### Assigning values to the Physical Constraint Set

In the Physical Constraint Set / All layers entry, the values can be assigned to the properties for the constraint set. The Constraint Sets will be named POWER, SYNC and VDNET as shown in the next figure, right-click on the DEFAULT entry in the worksheet and use Create - Physical CSet, specify a name for the new Constraint Set, the initial values will be copied from DEFAULT. In this case, Net Class members assigned the POWER Constraint Set will be routed at 0.5mm and necked to 0.2mm to allow for connections to smaller component pins. The Net Class members assigned the SYNC and VDNET Constraint Sets will be routed at 0.2mm and 0.3mm respectively.
Assigning the Physical Constraint Sets
Once created, the Physical Constraint Sets can be assigned to the Net Classes by selecting the required Physical Constraint Set from the drop-down list in the Referenced Physical CSet column, in the Net / All Layers entry.

(In this case, the names of the Net Classes and Physical Constraint Sets are very similar but this is not a requirement of PCB Editor)

Checking the Spacing Net Classes in PCB Editor
In the Spacing domain, left-click on the Spacing entry at the left hand side, go to the Net / All layers /Line and see that the Spacing classes have been applied:

Assigning values to the Spacing Constraint Set
In the Spacing Constraint Set / All Layers entry, open the "+" next to All Layers and locate the All at the bottom of the list. Then right-click on the DEFAULT entry and use Create - Spacing CSet, specify a name for the New Spacing Constraint Set, the initial values will be copied from DEFAULT. In this case the Spacing Constraint Sets will be called OUTPUT and SYNC and have 0.2mm and 0.3mm assigned to all the property entries. The Constraint Manager worksheets have behaviour similar to regular spreadsheets so, to assign the same value to all the property entries, select the first cell, you may need to click in the cell and use the arrow keys to move to the next cell and back to the first to get the cell boundary highlighted, as shown:
Then use the control / shift / right-arrow keyboard combination to get to the rightmost cell, then the shift / left-arrow keyboard combination to move left one cell to get all the editable cells selected. (So that the Min BB Via Gap is not selected). Then type the required value and enter. All the selected cells will be changed in one go. (The Min BB Via Gap can only be edited from the BB Via gap entry).

Assigning the Spacing Constraint Sets
Once created, the Spacing Constraint Sets can be assigned to the Net Classes by selecting the required Spacing Constraint Set from the drop-down list in the Referenced Spacing CSet column, in the Net / All Layers entry.

Creating a Differential Pair
The DSN file is selected in the Project Window and then Tools – Create Differential Pair, the following GUI will appear. You can manually select the two nets you wish to create a diff pair for select the forward arrow key and then specify a name (a default on is used in this example) then click on Create. DP1 is created.
If you have multiple differential pairs to create that have similar positive and negative naming conventions (diff1+ and diff1- or diff1_n and diff1_p for example) then it is recommended that you use the Auto Setup option, click on the Auto Setup button, define the + and – filters so that the appropriate nets are used, you can add a Prefix to the differential pair names (DP_ for example), then click on Create. For this example seven differential pairs are created.

Once netlisted into PCB Editor a look at the Constraint Manager – Electrical – Net – Routing – Differential Pair you can see the eight differential pairs. Rules can now be applied to the differential pairs. For further information on differential pairs please refer to Parallel Systems User Guide – How to Define Differential Pairs.

System Defined Netgroups (Bus)
Many designs today use buses to group nets together. Examples like PCI, DDR2 and 3 are becoming common. Capture allows users to create Netgroups which are transferred into PCB Editor as a system designed Bus so that electrical, physical and spacing rules can be applied. Netgroups can be created and then exported as xml files so they can be re-used again.

To create a Netgroup use the shortcut key U or Place – Netgroup. A GUI will appear that allows you to define the Netgroup names and net members.
To add a new Netgroup click on Add Netgroup, in the GUI specify a Netgroup name (DDR3 for example) and click on Apply. You now use the Add button to add the Netgroup members. These can be Netgroups, Buses or Scalar (single nets). Click OK to add the Netgroup member. Continue until the Netgroup definition is complete. Buses follow the default naming convention i.e. NAME[LSB..MSB] or NAME[LSB-MSB]

Once complete the GUI will look similar to:-

Click OK to confirm the Netgroup definition. The Netgroup is now available to be used.
Using Netgroups in an OrCAD Capture design.

If the Netgroup GUI is open select the Netgroup you wish to use and click OK. The mouse cursor changes from the default arrow to a crosshair (same behaviour when drawing bus). Draw where you want the Netgroup to be. You are drawing a Netgroup the same way you would draw a bus. Once complete you may have something similar to

The display of a Netgroup is graphically different to that of a bus. The line is thicker. The colour can be controlled in the Options – Preferences – Colors tab. Connect to the Netgroup as you would a bus. Since 16.5 there an auto-wire functions that connect to the bus/Netgroup is a more efficient way. For example Window select a group of pins that you wish to join to the Netgroup then RMB – Connect to Bus

Then select the Netgroup you wish to join to with a left click, the wires are drawn and you are given an option to select the Netgroup members you wish to use.

Select the relevant nets and click OK. The nets are named NETGROUPNAME.NETNAME as shown below.
To connect single pins to the bus select the pin then RMB – Connect to Bus, select the bus and the pick the netname from the GUI.

To use Netgroups across pages or between hierarchies use Off Page Connectors or Hierarchical ports as you would normally but ensure that you select a new checkbox for Netgroup OffPage or Netgroup Port. You can also select the specific Netgroup you wish to use from the dropdown.
Once your design is complete, netlist as you would normally. To view the Bus in PCB Editor open Constraint Manager – Physical (Spacing or Electrical) – Nets – All Layers then expand the + sign next to the Bus DDR3[0..20] (21) where 21 is the number of members in the bus.

Rules can be applied as stated earlier.